REMARKS

Claims 1-20 are pending in the present application. Claims 1-4 are independent. Dependent claims 5-20 have been added. Support for the added dependent claims 5-20 may be found, *inter alia*, in FIG. 1 and pages 5 and 6 of the specification.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Surlekar. Applicant respectfully traverses.

Surlekar discloses a testing apparatus that tests memory. The testing procedure associated with the testing apparatus involves storing a selected logic signal, referred to as an expected data signal. The procedure further involves retrieving the stored logic signal from each storage cell in memory, and comparing the retrieved data signals with the expected data signal. This is done to verify that the storage into and retrieval from the storage cells provides the signal that was originally stored in the memory unit (Col. 2, lines 37-44). To accomplish this, the Surlekar apparatus needs a certain type of memory to test as shown in FIG. 1.

FIG. 1 discloses a memory device that the Surlekar testing apparatus may test. The memory shows a Data Input/Output Buffer 16 that receives information from a Memory Array 15 and data input from a Data In Register 18, and outputs information through a Data Out Register 17.

With regard to independent claims 1 and 2, Applicant asserts that Surlekar fails to disclose a data output buffer for transferring internal signals to outside of a device through data input/output pads; wherein the internal signals are used for addressing storage locations and for controlling internal operations as recited in claims 1 and 2.

The Examiner suggests that Surlekar discloses, in FIG. 1, a Data Output Buffer 16 and a Data Out Register 17 that are the same as the data output buffer and input/output pads as recited in claims 1 and 2. Applicant respectfully disagrees.

With regard to independent claims 1 and 2, a data output buffer transfers internal signals external to an integrated circuit device through data input/output pads. Surlekar only transfers data to the Data Input/Output Buffer 16 and the Data Out Register 17 as shown in FIG. 1 and is silent as to internal signals output through a data input/output pad as recited in claims 1 and 2. While Surlekar does disclose the output of data through its Data Output Buffer 16 and Data Out Register 17, this data is different than the internal signals of independent claims 1 and 2. The internal signals of independent claims 1 and 2 are used for addressing storage locations and for controlling internal operations. The Surlekar data is data that is stored in a memory, retrieved, and then compared as disclosed at Col. 2, lines 37-44. The Surlekar data is not used for addressing storage locations and for controlling internal operations. Thus, Surlekar fails to disclose a data output buffer that transfers internal signals external to an integrated circuit device through data input/output pads as recited in claims 1 and 2.

With regard to independent claims 3 and 4, Applicant asserts that Surlekar fails to disclose a data output buffer for transferring internal signals external to a device through data input/output pads as recited in claims 3 and 4.

The Examiner suggests that Surlekar discloses, in FIG. 1, a Data Output Buffer 16 and a Data Out Register 17 that are the same as the data output buffer and input/output pads as recited in claims 3 and 4. Applicant respectfully disagrees.

With regard to independent claims 3 and 4, a data output buffer transfers internal signals external to an integrated circuit device through data input/output pads. Surlekar only transfers data

to the Data Input/Output Buffer 16 and the Data Out Register 17 as shown in FIG. 1. Specifically, Surlekar, is silent as to internal signals output through a data input/output pad as recited in claims 3 and 4.

For at least these reasons, Applicant asserts that Surlekar fails to disclose each and every element of claims 1-4 as is required for a 35 U.S.C. 102. Accordingly, Applicant asserts that independent claims 1-4 are allowable, and respectfully requests that the 35 U.S.C. 102 rejection of claims 1-4 be withdrawn.

With regard to dependent claims 5-20, Applicant asserts that they are allowable for their own merits and at least because they depend from at least one of independent claims 1-4, which the Applicant believes have been shown to be allowable.

CONCLUSION

In view of the foregoing, Applicant submits that claims 1-20 are patentable, and that the application as a whole is in condition for allowance. Early and favorable notice to that effect is respectfully solicited.

In the event that any matters remain at issue in the application, the Examiner is invited to contact the undersigned at (703) 668-8000 in the Northern Virginia area, for the purpose of a telephonic interview.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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